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The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

**1. (Cancelled)**

**2. (Currently Amended):** A substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel **having a top surface and a bottom surface, the panel** including a plurality of device areas, each device area having a die attach pad and a plurality of contacts, wherein each die attach pad includes a die support surface and a uniform peripheral ledge that is recessed relative to the die support surface wherein the uniformly recessed peripheral ledges extend around the outer edges of the die attach pads**, wherein the die support surface is formed on the top surface and is coplanar with top surfaces of the plurality of contacts**; and

a plurality of semiconductor dice, each die being attached to the die support surface of an associated die attach pad using an adhesive, wherein a portion of each semiconductor die extends beyond an outer edge of its associated die attach pad, and wherein the ledge is configured to retain an amount of the adhesive.

**3. (Currently Amended):** The substrate panel of claim 2 wherein ~~**each die attach pad has a second surface opposite to the die attach surface, wherein**~~ **the devices areas are sized so that** the area of the die attach surface **formed on the top surface** is less than the area of the **bottom surface of the die attach pad** ~~**second surface**~~.

**4. (Previously Presented):** A substrate panel as recited in claim 2 wherein bottom surfaces of the contacts are substantially co-planar with bottom surfaces of the die attach pads.

**5. (Original):** A substrate panel as recited in claim 4 further comprising an encapsulant applied to the lead frame panel, wherein the second surfaces of the die attach pads and the bottom surfaces of the contacts are exposed on an outer surface of the encapsulant, and wherein the peripheral ledges retain amounts of the adhesive so as to prevent the adhesive from being exposed on the outer surface of the encapsulant.

**6. (Previously Presented):** The substrate panel of claim 2 wherein at least some of the semiconductor dice are down bonded to the respective ledges of their associated die attach pads.

**7. (Previously Presented):** The substrate panel of claim 2 wherein the lead frame panel comprises a matrix of tie bars arranged in perpendicular rows and columns that define a two dimensional array of the device areas such that adjacent device areas are separated only by the tie bars.

**8. (Cancelled)**

**9. (Currently Amended):** A packaged integrated circuit, comprising:

a substrate **having a top surface and a bottom surface, the substrate** having a die attach pad and a plurality of contacts, the die attach pad **top surface includes** ~~having an upper surface and~~ a uniformly recessed peripheral ledge located proximate to, and surrounding, an outer edge of the **top** [[upper]] surface and configured such that the uniformly recessed peripheral ledge extends to an outer edge of the die attach pad, **wherein the top surface of the die attach pad is coplanar with top surfaces of the plurality of contacts;**

a semiconductor die mounted on the **top surface** ~~upper surface~~ with an adhesive;

wherein a portion of the die extends beyond an outer edge of the **top surface** ~~upper surface~~; and

wherein the peripheral ledge is configured to retain a portion of the adhesive so as to inhibit a flow of the adhesive from the die attach pad.

**10. (Currently Amended):** The integrated circuit of claim 9 wherein ~~the die attach pad has a lower surface opposite to the upper surface,~~ the peripheral ledge **is** configured so that the area of the ~~upper~~ **top** surface **of the die attach pad smaller than a bottom surface of the die attach pad.** ~~is less than the area of the lower surface.~~

**11. (Previously Presented):** The integrated circuit of claim 9 wherein bottom surfaces of the contacts are substantially co-planar with bottom surfaces of the die attach pad.

**12. (Original):** The integrated circuit of claim 11 further comprising an encapsulant applied to the substrate and the semiconductor die, wherein a lower surface of the die attach pad is exposed on an outer surface of the encapsulant, and wherein the peripheral ledge retains an

amount of the adhesive so as to prevent the adhesive from being exposed on the outer surface of the encapsulant.

**13. (Previously Presented):** The integrated circuit of claim 9 wherein the die is down bonded to the peripheral area.

**14-15. (Cancelled)**

**16. (Currently Amended):** A substrate panel for use in semiconductor packaging, the substrate panel comprising:

a lead frame panel **having a top surface and a bottom surface, the panel** including a plurality of device areas, each device area having a plurality of contacts arranged around a die attach pad, wherein each die attach pad includes a die support surface and a recessed ledge portion that is lower than die support surface and extends uniformly to an edge of the die attach pad, **the panel is further configured so that the top surface of the die attach pad and the top surfaces of the plurality of contacts are substantially coplanar**.

**17. (Previously Presented):** The substrate panel of claim 16 wherein the peripheral recessed ledge portions extend uniformly around all of the outer edges of the die attach pads.

**18. (Previously Presented):** The substrate panel of claim 17 wherein a plurality of semiconductor dice are attached to the die support surface of each die attach pad using an adhesive layer, wherein a portion of each semiconductor die extends beyond an outer edge of its associated die attach pad, and wherein the ledge portion is configured to retain an amount of the adhesive.

**19. (Previously Presented):** The substrate panel of claim 18 wherein each of the semiconductor dies are electrically connected with the plurality of contacts arranged around the die and wherein each die and associated electrical connections to the contacts are encapsulated.

**20. (New):** The substrate panel of Claim 2 wherein the die support surfaces are adapted to receive semiconductor die in a manner so that for each device area a bottom surface of a die is adhered to the top surface of the panel at the die support surface, and wherein the opposing top surface of the die is wired bonded to the plurality of contacts of the device area so that a wire

connection extends from the top surfaces of the plurality of contacts to the top surface of the die to form a wire bonded connection.

21. (New): The packaged integrated circuit of Claim 9 wherein a bottom surface of the semiconductor die is mounted to the top surface of the substrate with the adhesive and wherein a top surface of the die is wired bonded to the plurality of contacts of the substrate so that a wire connection extends from the top surfaces of the plurality of contacts to the top surface of the die to form a wire bonded connection.

22. (New): The substrate panel of claim 19 wherein a top surface of each of the semiconductor dies are electrically connected with the top surface of the plurality of contacts by wired bonded electrical connections that are wire bonded to the top surface of the dies and to the top surface of associated contacts.